REMARKS

This communication is responsive to the Office Action mailed on September 30, 2004. No claims are amended, no claims are canceled, and no claims are added. As a result, claims 7-26 are now pending in this Application.

If the Examiner is not convinced that the pending claims are in condition for allowance after reviewing this document, the courtesy of an Examiner's Interview is respectfully requested prior to preparing and mailing any Final Office Action.

Objection to the Abstract

An objection was raised to the Abstract of the Disclosure as being directed to a non-elected invention. Without prejudice or disclaimer, the Abstract of the Disclosure has now been amended to more fully incorporate various features of the claimed embodiments. Should further amendment be necessary, the Applicants would be pleased to rely on the Examiner for guidance in this matter, and actively solicit the comments of the Examiner in this regard. Finally, it should be noted that the amended Abstract of the Disclosure is provided so as to comply with 37 C.F.R. §1.72(b), requiring an abstract that will allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims.

Double Patenting Rejection

Claims 7-26 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 26-37 of co-pending U.S. Patent Application Serial No. 10/146,689. The Applicants respectfully note that U.S. Patent Application Serial No. 10/146,689 has now issued as U.S. Patent No. 6,812,757. A Terminal Disclaimer in compliance with 37 CFR 1.321(b)(iv) is enclosed herewith to obviate the rejection.

§103 Rejection of the Claims

Claims 7-11 and 17-26 were rejected under 35 USC § 103(a) as being unpatentable over Soyuer (U.S. 5,422,603; hereinafter "Soyuer") in view of Matsui (U.S. 6,300,803; hereinafter

"Matsui"). Claims 12-16 were also rejected under 35 USC § 103(a) as being unpatentable over Ishikawa (U.S. 5,748,018; hereinafter "Ishikawa") in view of Soyner and Matsui. First, the Applicants do not admit that Soyuer, Matsui, or Ishikawa are prior art, and reserve the right to swear behind these references in the future. Second, since a *prima facie* case of obviousness has not been established as required by M.P.E.P. § 2142, the Applicants respectfully traverse this rejection.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.* The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference. *In re Oetiker*, 977 F.2d 1443, 24 U.S.P.Q.2d (BNA) 1443 (Fed. Cir. 1992). However, while it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 U.S.P.Q.2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 U.S.P.Q. 171, 174 (C.C.P.A. 1979)). The requirement of a suggestion or

motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which notes that the motivation must be supported by evidence in the record.

No proper *prima facie* case of obviousness has been established in this case because (1) there is no motivation to combine the references, (2) there is no reasonable expectation of success if the references are combined, and (3) any combination of the references does not teach all the limitations set forth in the claims. Each of these points will be explained in detail, as follows.

There Is No Motivation to Combine the References. FIG. 1 of Soyuer illustrates a CMOS synthesizer including a phase frequency detector (PFD) 300 coupled to a voltage controlled oscillator (VCO) 100 having two control inputs. See Soyuer, Col. 2, lines 20-30. Matsui teaches a phase-comparison circuit in FIG. 8 that operates by converting two voltage signals Vin1 and Vin2 at the input into a single output, the current Iout, representing the difference in phase between the two input voltages. See Matsui, Col. 1, lines 5-8, and Col. 7, lines 3-8 and 39-58.

With respect to claims 7-11 and 17-26, it is asserted in the Office Action that "it would have been obvious ... to use the specific [phase-comparison] circuit of Matsui for the broad phase detector 300 of Soyuer for the expected advantage of offset compensation." It is also alleged that "Soyuer fails to disclose any specific details for the broad phase detector 300." However, Soyuer does teach several elements required by the VCO 100 (and provided by the broad phase detector 300) for proper operation. These elements are not (and can not be) provided by the phase-comparison circuit of Matsui.

The VCO 100 of Soyuer is controlled using two separate output signals derived from the PFD 300. Soyuer, Col. 2, lines 28-32. As can be seen in FIG. 2 of Soyuer, the PFD 300 is a fully symmetric PFD. It is the "fully symmetric architecture ... [that] minimizes the effect of the dead-zone on PFD performance." See Soyuer, Col. 4, lines 9-12. According to Soyuer, "the UP or DN outputs and their complements, UPB or DNB .... [have] duty cycles [that] are proportional to the phase and frequency difference between the inputs R/RB and V/VB." Soyuer, Col. 3, lines 61-64. Thus, the PFD 300 of Soyuer provides two outputs to the VCO 100: one for the difference in phase (similar to Iout of Matsui), and the other *for the difference in*

frequency. The VCO 100 requires *both* of these control signals, processed through parallel delay lines of different lengths, to function properly. Soyuer, Col. 2, lines 28-43. In other words, if the VCO 100 of Soyuer does not receive both *phase and frequency* control inputs (e.g., as supplied by Soyuer's PFD 300), it will not operate. Matsui does not provide the needed frequency difference output.

To modify Soyuer to use the phase-comparison circuit of Matsui renders Soyuer inoperable, since this combination would attempt to control a dual-input phase/frequency VCO (Soyuer) using the single, phase-only output provided by Matsui. The single output (Iout) of Matsui's phase-comparison circuit is not symmetric, and would not allow the charge-pump filter of Soyuer to provide a differential output, which is "exactly what is required to reduce the susceptibility of the charge pump to crossover distortion for small phase differences between the PFD input signals." See Soyuer, Col. 5, 38-41. In other words, attempting to operate the VCO 100 of Soyuer using the single output of Matsui's phase-comparison circuit fails to provide the *frequency difference information* required for proper operation of Soyuer's VCO 100.

The rejection of claims 12-16 also relies on the assumption of fundamental compatibility between Soyuer's VCO 100 and Matsui's phase comparison circuit. However, as noted previously, this combination is not operable. The addition of Ishikawa's phase lock loop 613 and elements 100, 200 does nothing to remedy the defective combination of Soyuer and Matsui.

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1143, 227 U.S.P.Q. (BNA) 543, 551 (Fed. Cir. 1985). If the proposed modification renders the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *M.P.E.P.* § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984)). The Examiner must also avoid hindsight. *Id.* The Examiner cannot use the Appellant's structure as a "template" and simply select elements from the references to reconstruct the claimed invention. *In re Gorman,* 933 F.2d 982, 987, 18 U.S.P.Q.2d (BNA) 1885, 1888 (Fed. Cir. 1991). Since modifying the VCO of Soyuer to make use of Matsui's phase-comparison circuit (that provides no frequency difference information) would render Soyuer's device inoperable, there is no motivation to combine these references.

Further, there is no evidence in the record to support the assertion by the Office that "it would have been obvious for one skilled in the art to use the specific [phase-comparison] circuit of Matsui for the broad phase detector 300 of Soyuer for the expected advantage of offset comparison." The asserted advantage of "offset compensation" offered in the Office Action is not noted as desirable by Soyuer, which specifically states that "It is the purpose of this invention to reduce jitter and improve synthesizer speed without the need for any technology other than CMOS." Soyuer, Col. 1, lines 31-34. This use of an unsupported assertion does not satisfy the explicit requirements set forth by the *In re Sang Su Lee* court. *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002) (motivation must be supported by evidence in the record). Thus, the Examiner appears to be using personal knowledge, and is thus respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

There Is No Reasonable Expectation of Success. Combining Soyuer and Matsui does not achieve or advance the goals of either system. Adding the phase-comparison circuit of Matsui (providing a single, phase-only output) to Soyuer's dual-input phase/frequency VCO takes away the advantage of Soyuer's design to minimize "the high-speed mismatch effects from the switching speeds and bias currents of NMOS and PMOS devices." See Soyuer, Col. 5, lines 34-38.

Similarly, Matsui is directed to providing a current mirror within a phase-comparison circuit to compensate for errors between a reference current and an output current. See Matsui, Col. 3, lines 39-44. The circuitry of Soyuer, dealing with differential voltages, does nothing to assist in this endeavor. Thus, combining Soyuer and Matsui does not convey a reasonable expectation of success in either case.

As noted previously, the rejection of claims 12-16 relies on the assumption of fundamental compatibility between Soyuer's VCO 100 and Matsui's phase comparison circuit. However, this combination is not operable, and the addition of Ishikawa's phase lock loop 613 and elements 100, 200 does nothing to transform the combination of Soyuer and Matsui into an apparatus capable of successful operation.

The References Do Not Teach All Claim Limitations. The PFD 300 of Soyuer does not include a "voltage-to-current circuit to influence a voltage on a capacitor" and a "voltage controlled oscillator responsive to the voltage on the capacitor" as claimed by the Applicants in

independent claims 7 and 12 (and in dependent claims 8-11, 13-16, and 23-26). Nor does Soyuer include a "voltage controlled oscillator to generate a differential signal on two nodes", a "sampling circuit to periodically sample voltage values on the two nodes" and a "linear voltage-to-current converter responsive to the voltage values to create a control voltage for the voltage controlled oscillator" as claimed by the Applicants in independent claim 17 (and in dependent claims 18-22).

In addition, niether Matsui nor Ishikawa discloses a "voltage-to-current circuit to influence a voltage on a capacitor" and a "voltage controlled oscillator responsive to the voltage on the capacitor" as claimed by the Applicants in 12 (and in dependent claims 13-16). In fact, Matsui's phase comparison circuit is current-based. Therefore, no combination of Soyuer, Matsui, or Ishikawa can provide these missing elements.

Thus, a *prima facie* case of obviousness has not been established by the combination of Soyuer, Matsui, or Ishikawa. There is no motivation to combine the references (in fact, the references teach away from such a combination), there is no reasonable expectation of success if the references are combined, and any combination of the references would not teach all of the limitations in the claims. Therefore, it is respectfully asserted that no proper combination of Soyuer, Matsui, or Ishikawa can be made to disclose the embodiments claimed, and it is respectfully requested that the rejection of claims 7-26 under 35 U.S.C. §103 be reconsidered and withdrawn.

CONCLUSION

The Applicants respectfully submit that all of the pending claims are in condition for allowance and notification to that effect is earnestly requested. As noted above, if the Examiner is not convinced that all of the pending claims are in condition for allowance after reviewing this document, the courtesy of an Examiner's Interview is respectfully requested prior to preparing and mailing any Final Office Action.

The Examiner is invited to telephone the Applicants' attorney Mark Muller at (210) 308-5677, or the undersigned attorney to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date Nov. 30, 2004

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 30 day of November 2004.

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Signature